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EXAMINER
MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
2183	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/430,192	RAYNHAM ET AL.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Pending claims 1-10 have all been rejected two different ways. The first manner in which Examiner has rejected claims 1-10 appears below under the section heading "1st Set of Rejections" and the second manner in which Examiner has rejected claims 1-10 appears below under the section heading "2nd Set of Rejections."

1st Set of Rejections

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wirthlin et al., in view of Que, previously cited as a prior art reference in paper number 5 mailed on April 24, 2002, and Page.

4. Referring to claim 1, Wirthlin et al. have taught a subsystem controller for control of a device or subsystem within an electronic system having system processing components (Abstract, Figures 1-9) , the subsystem controller comprising:

a. a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality (page 1, Abstract, Introduction);

b. a micro-controller that can execute software routines that implement control functionality (page 1, Abstract, Introduction, "general purpose processor");

c. random-access memory that can store data and executable code for execution by the micro-controller (Figure 7, SRAM and DRAM);

d. a bus interface for exchanging data and control signals between the subsystem controller and system processing components (Figure 7, See the connection from the Xilinx 3090 to the PC Interface.); and

e. an additional electronic interface to a device or subsystem controlled by the subsystem controller (Figure 7, See the connection from the Xilinx 3090 to the MIDI and the connection from the Xilinx 3090 to the ADC DAC.).

5. Wirthlin et al. have not taught read-only memory that stores executable code for execution by the micro-controller. However, Que has taught utilizing ROM in place of the random-access memory (RAM) to store executable code to be run on the micro-controller would have allowed for the system to retain such code in the system power-off state and load the code immediately upon a change to power-up (Que page 416). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize read-only memory, or ROM, to store executable code for execution by the micro-controller as taught by Que instead of the random-access memory, or RAM, of Page, in order to ensure immediate loading of the code upon system power-up.

6. Wirthlin et al. have also not taught that the subsystem controller is implemented as a single integrated circuit. However, Page has taught that combining a programmable logic device and the processor on the same chip reduces the number of parts in a typical system and speeds up system communication (Figure 1, Wirthlin et al., pages 6 and 7, Section 6 entitled "Combining Processor and DPGA on the Same Chip"). It would have been obvious to one of ordinary skill in

the art at the time the invention was made to have the subsystem controller, as taught by Wirthlin et al., be implemented as an integrated circuit in order to speed up communication and reduce the number of parts, which reduces the cost of the overall system (Wirthlin et al., pages 6 and 7, Section 6 entitled "Combining Processor and DPGA on the Same Chip").

7. Referring to claim 2, Wirthlin et al. have taught the subsystem controller of claim 1, as described above, and wherein control functionality of the subsystem controller is partitioned between logic circuits programmed into the complex programmable logic device and software routines executed by the micro-controller (Wirthlin et al., page 2, section 2.2).

8. Referring to claim 4, Wirthlin et al. in combination with Que and Page have taught the subsystem controller of claim 1 wherein the bus interface is an 1^2C bus interface (The bus interface as taught by Wirthlin et al., Que, and Page must be by way of I^2C, or inter-integrated circuit buses such that any bus connecting 2 integrated circuits is an I^2C bus).

9. Referring to claim 5, The subsystem controller of claim 1 wherein the additional electronic interface is an 8-bit input/output bus and additional signal lines (Pages7-8, Section 4.1 Audio Interface).

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sudo, US Patent 6,047,198, previously cited as a prior art reference in paper number 5 mailed on April 24, 2002, in view of Wirthlin et al., Que, previously cited as a prior art reference in paper number 5 mailed on April 24, 2002, and Page. Sudo has taught a controller programmed to display information (Sudo figure 4, element 5A) on an LCD display window included in an external front panel display of a server computer (Sudo figures 3 and 4, element 5 and figures 8A-J). Sudo has further taught a general-purpose CPU (Sudo figure 4, element 7) to control the entire system.

Sudo has not taught the subsystem controller as in claim 1. However, as has been described in the rejection to claim 1 above, Wirthlin et al. in combination with Que and Page have taught each and every limitation of claim 1. An artisan would have been motivated to employ the system of Wirthlin et al., Que, and Page, as the CPU of Sudo, where the complex programmable logic device is used as an input/output controller, in this case the LCD controller. Using the complex programmable logic device/micro-controller IC system would have allowed for less glue logic such that the LCD control would have been part of the overall system control, or CPU, rather than extra, external circuitry. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the IC subsystem controller of Wirthlin et al., Que, and Page within the system of Sudo in order to decrease the amount of hardware required and make the overall system more cost-effective and lighter.

11. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wirthlin et al., in view of Que, previously cited as a prior art reference in paper number 5 mailed on April 24, 2002, and Page.

12. Referring to claim 6, Wirthlin et al. have taught a method for controlling a subsystem within a complex electrical device, the method comprising:

a. providing a subsystem controller (Figure 7, The MIDI and the ADCDAC are both subsystems controlled by the subsystem controller.);

b. programming control functionality into the subsystem controller by

i. programming logic circuits into a complex programmable logic device included in the subsystem controller (Abstract, page 1, section 1, Introduction page 2, Sections 2.1 and 2.2.),

ii. implementing software routines for execution by a micro-controller within the single-IC subsystem controller (Abstract, page 1, section 1Introduction page 2, Sections 2.1 and 2.2.), and

iii. storing the software routines in the subsystem controller (Figures 1, 2, and 7, SRAM, page 7, last full paragraph); and

c. interconnecting the subsystem controller to the subsystem within the complex electrical device (Figures 7 and 8, See the connection from the Xilinx 3090 to the MIDI and the connection from the Xilinx 3090 to the ADC DAC).

13. Wirthlin et al. have not specifically taught that the subsystem controller is a single-IC. However, Page has taught that combining a programmable logic device and the processor on the same chip reduces the number of parts in a typical system and speeds up system communication (Figure 1, Wirthlin et al., pages 6 and 7, Section 6 entitled "Combining Processor and DPGA on the Same Chip"). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the subsystem controller, as taught by Wirthlin et al., be implemented as a single-IC in order to speed up communication and reduce the number of parts, which reduces the cost of the overall system (Wirthlin et al., pages 6 and 7, Section 6 entitled "Combining Processor and DPGA on the Same Chip").

14. Referring to claim 8, Witthlin et al have taught the method of claim 6, as described above, and wherein the complex electrical device is a computer system (pages 6-8).

15. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sudo, US Patent 6,047,198, previously cited as a prior art reference in paper number 5 mailed on April 24, 2002, in view of Wirthlin et al. and Page. Sudo has taught a method including a complex electrical

device, wherein a controller is programmed to display information (Sudo figure 4, element 5A) on a subsystem, i.e. an LCD display window (Sudo figures 3 and 4, element 5) that displays information about the components and state of the complex electrical device (Sudo figures 8A-J). Sudo has further taught a general-purpose CPU (Sudo figure 4, element 7) to control the entire system. Sudo has not taught the subsystem controller as in claim 6. However, as has been described in the rejection to claim 6 above, Wirthlin et al. and Page have taught each and every limitation of claim 6. An artisan would have been motivated to employ the system of Wirthlin et al., Que, and Page, as the CPU of Sudo, where the complex programmable logic device is used as an input/output controller, in this case the LCD controller. Using the complex programmable logic device/micro-controller IC system would have allowed for less glue logic such that the LCD control would have been part of the overall system control, or CPU, rather than extra, external circuitry. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the IC subsystem controller of Wirthlin et al., Que, and Page within the system of Sudo in order to decrease the amount of hardware required and make the overall system more cost-effective and lighter.

16. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wirthlin et al., in view of Que, previously cited as a prior art reference in paper number 5 mailed on April 24, 2002, and Page.

17. Referring to claim 9, Wirthlin et al. have taught the method of claim 6, as described above, and wherein the single-IC subsystem controller includes the complex programmable logic device (page 1, Abstract, Introduction), the micro-controller (page 1, Abstract, Introduction, "general purpose processor"), a random-access memory (Figure 7, SRAM and DRAM), a bus

interface (Figure 7, See the connection from the Xilinx 3090 to the PC Interface.), and an additional electronic interface (Figure 7, See the connection from the Xilinx 3090 to the MIDI and the connection from the Xilinx 3090 to the ADC DAC.).

18. Wirthlin et al. have not taught that the single-IC subsystem controller includes a read-only memory. However, Que has taught utilizing ROM in place of the random-access memory (RAM) to store executable code to be run on the micro-controller would have allowed for the system to retain such code in the system power-off state and load the code immediately upon a change to power-up (Que page 416). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize read-only memory, or ROM, to store executable code for execution by the micro-controller as taught by Que instead of the random-access memory, or RAM, of Page, in order to ensure immediate loading of the code upon system power-up.

19. Referring to claim 10, Wirthlin et al. have taught the method of claim 9, as described above, and wherein interconnecting the single-IC subsystem controller to the subsystem within the complex electrical device further includes interconnecting the subsystem with the additional electronic interface (Figure 7, See the connection from the Xilinx 3090 to the MIDI and the connection from the Xilinx 3090 to the ADC DAC.).

2nd Set of Rejections

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huffener, US Patent 5,382,891 in view of Wirthlin et al.

22. Referring to claim 1, Huffener has taught a subsystem controller implemented as a single integrated circuit for control of a device or subsystem within an electronic system having system processing components (Figure 12), the subsystem controller comprising:

a. a micro-controller that can execute software routines that implement control functionality (Figure 12, column 10, lines 9-57);

b. random-access memory that can store data and executable code for execution by the micro-controller (Figure 12, column 10, lines 9-57, 256 byte RAM);

c. a bus interface for exchanging data and control signals between the subsystem controller and system processing components (Figure 12, column 10, lines 9-column 11, line 32, MIDI bus interface); and

d. an additional electronic interface to a device or subsystem controlled by the subsystem controller (Figure 12, column 10, lines 9-column 11, line 32, LCD display).

23. Huffener has not taught the subsystem controller comprises a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality. Wirthlin et al. have taught a subsystem controller that comprises a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality (Wirthlin et al., Page 1, Abstract). It would have been obvious to one of ordinary skill in the art a the time the invention was made to include the complex programmable logic device that can be programmed to provide logic circuits that implement control

functionality, as taught by Witthlin et al., into the subsystem controller of Huffener, for the desirable purpose of creating a more flexible and reconfigurable microcontroller with a relatively small amount of development time (Wirthlin et al., Page 1, Abstract).

24. Huffener has taught a ROM memory that stores executable code for execution by the microcontroller (Figure 12, element 87, column 10, lines 21-27). Huffener has not taught that the read-only memory is included in the subsystem controller implemented as a single integrated circuit. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the ROM on chip in order to reduce the amount of parts needed in a typical system and speed up communication time from the ROM to the microprocessor. (See Page) Furthermore, making the ROM integral to the integrated circuit is not a patentable difference as it has been held that making something integral is not a patentable difference. See *In re Larson*, 340F.2d 965, 967, 144 USPQ 347, 349 (CCPA 1965); *In re Wolf*, 251 F.2d 854, 855, 116 USPQ 443, 444 (CCPA 1958).

25. Referring to claim 2, Huffener in combination with Wirthlin et al. have taught the subsystem controller of claim 1, as described above, and wherein control functionality of the subsystem controller is partitioned between logic circuits programmed into the complex programmable logic device and software routines executed by the micro-controller (Wirthlin et al., page 2, section 2.2).

26. Referring to claim 3, Huffener in combination with Wirthlin et al. have taught the subsystem controller of claim 1 programmed to control display of information on an LCD display window included in an external front panel display of a server computer (Huffener, Figure 12, element 92, column 10, lines 54-57).

27. Referring to claim 4, Huffener in combination with Wirthlin et al. have taught the subsystem controller of claim 1, as described above, and wherein the bus interface is an 1^2C bus interface (The bus interface as taught by Huffener must be by way of I^2C, or inter-integrated circuit buses such that any bus connecting 2 integrated circuits is an I^2C bus.).

28. Referring to claim 5, Huffener in combination with Page have taught the subsystem controller of claim 1 wherein the additional electronic interface is an 8-bit input/output bus and additional signal lines (Huffener, column 10, lines 54-57).

29. Referring to claim 6, Huffener have taught a method for controlling a subsystem within a complex electrical device, the method comprising:

a. providing a single-IC subsystem controller (Figure 12, element 85, column 10, line 9-column 11, line 54);

b. programming control functionality into the single-IC subsystem controller by implementing software routines for execution by a micro-controller within the single-IC subsystem controller (column 10, line 9-column 11, line 32); and

c. interconnecting the single-IC subsystem controller to the subsystem within the complex electrical device (Figure 12, column 10, lines 9-column 11, line 32, LCD display).

30. Huffener has not taught specifically taught programming control functionality into the single-IC subsystem controller by programming logic circuits into a complex programmable logic device included in the single-IC subsystem controller. Wirthlin et al. have taught programming control functionality into the single-IC subsystem controller by programming logic circuits into a complex programmable logic device included in the single-IC subsystem

controller (Wirthlin et al., Page 1, Abstract). It would have been obvious to one of ordinary skill in the art a the time the invention was made to program control functionality into the single-IC subsystem controller by programming logic circuits into a complex programmable logic device included in the single-IC subsystem controller, as taught by Witthlin et al., into the subsystem controller of Huffener, for the desirable purpose of creating a more flexible and reconfigurable microcontroller with a relatively small amount of development time (Wirthlin et al., Page 1, Abstract).

31. Huffener has not specifically taught storing the software routines in the single-IC subsystem controller. However Huffener has taught a ROM memory that stores executable code for execution by the microcontroller (Figure 12, element 87, column 10, lines 21-27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the ROM on chip in order to reduce the amount of parts needed in a typical system and speed up communication time from the ROM to the microprocessor. Furthermore, making the ROM integral to the integrated circuit is not a patentable difference as it has been held that making something integral is not a patentable difference. See *In re Larson*, 340F.2d 965, 967, 144 USPQ 347, 349 (CCPA 1965); *In re Wolf*, 251 F.2d 854, 855, 116 USPQ 443, 444 (CCPA 1958).

32. Referring to claim 7, Huffener in combination with Wirthlin et al. have taught the method of claim 6, as described above, and wherein the subsystem is an LCD display window that displays information about the components within the complex electrical device and about the state of the complex electrical device (Huffener, Figure 12, element 92, column 10, lines 54-57).

33. Referring to claim 8, Huffener in combination with Wirthlin et al. have taught the method of claim 6, as described above, and wherein the complex electrical device is a computer system (Huffener, Column 10, line 9-column 11, line 32).

34. Referring to claim 9, Huffener in combination with Wirthlin et al. have taught the method of claim 6, as described above, and wherein the single-IC subsystem controller includes the complex programmable logic device (Wirthlin et al., page 1, abstract, see rejection to claim 6), the micro-controller (Huffener, Column 10, line 9-column 11, line 32), a read-only memory (Huffener, Column 10, line 9-column 11, line 32, EPROM, see rejection to claim 6), a random-access memory (Huffener, Column 10, line 9-column 11, line 32, 256 byte RAM), a bus interface (Figure 12, column 10, lines 9-column 11, line 32, MIDI bus interface), and an additional electronic interface (Figure 12, column 10, lines 9-column 11, line 32, LCD display).

35. Referring to claim 10, Huffener in combination with Wirthlin et al. have taught the method of claim 9, as described above, and wherein interconnecting the single-IC subsystem controller to the subsystem within the complex electrical device further includes interconnecting the subsystem with the additional electronic interface (Huffener, Figure 12, column 10, lines 9-column 11, line 32, LCD display).

Response to Arguments

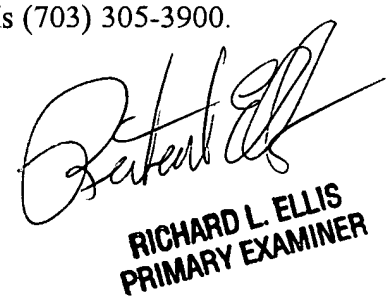
36. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

39. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.



tlm
May 1, 2003